Jointly Organized by
Electronics & ICT Academies

MNITJ, IITG, NITP, IIITDMJ, IITR
http://www.mnit.ac.in/eict

Online Programme
on
Foundations of VLSI Design Verification

23rd June – 6th July 2025

Faculty Development Programme
Electronics & ICT Academy under aegis of

Ministry of Electronics and Information Technology
Government of India

meity.gov.in/content/schemes-projects

Chairman, EICT Academy &
Director MNIT Jaipur
Prof. Narayana Prasad Padhy

Chief Investigator, EICT Academy
Prof. Vineet Sahula, ECE

Coordinator, EICT Academy
Dr. Satyasai Jagannath Nanda, ECE

Co- Chief Investigators, EICT Academy
Prof. Lava Bhargava, ECE
Prof. Pilli Emmanuel Shubhakar, CSE
Dr. Ravi Kumar Maddila, ECE

Objective (Electronics & ICT Academy-Phase II)
1)To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.
2) To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.
3) To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India AI; National Programme on AI, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.
4) To promote standardization of FDPs through Joint Faculty Development Programmes.
5) To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.
6) To design, develop & deliver specialised FDPs on emerging technologies/ niche areas/ specialised modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multi-disciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of engineering and non-engineering colleges, polytechnics, ITIs, and PGT educators.

An intensive 40 Hours Training Programme will be offered in online mode and is intended for faculty and doctoral students of engineering and technological institutions. The training program will explore the theme of **Foundations of VLSI Design Verification** which is a skill in high demand in the VLSI/semiconductor industry. The classes will be held during **7 - 9 PM (workdays) and 5 hours each on Saturday and Sunday**.

Instructor: Dr. C.P. Ravikumar served in Texas Instruments (India) for 23 years in roles such as the Director of Technical Talent Development and Director of University Relations. He served as a Professor of Electrical Engineering at IIT Delhi for 10 years. He is currently the Chief Learning Officer at Vinyana Tech.

Programme Modules:

- Introduction to Design Verification
- Functional Simulation as a Verification Tool
- Testbench Development
- Sequential Circuit Verification
- Verilog Testbench Concepts
- Introduction to SystemVerilog as a Hardware Verification Language (HVL)
- Object-Oriented Programming in SystemVerilog
- Advanced Verification Techniques
- Comprehensive System Verification Example
- Industry Practices and Career Insights

Methodology:

- Lectures: Conceptual understanding and theoretical foundations
- Hands-on Labs: Practical application through guided exercises
- Mini Project: Integration of learned concepts in a comprehensive verification task
- Course materials will be provided during the course.

Prerequisites:

- Basic knowledge of digital design principles
- Familiarity with Verilog is beneficial but not mandatory

Principal Coordinators:

Prof. Vineet Sahula, MNIT Jaipur 954 9654 227 (M)	fdp.academy@mnit.ac.in	Dr. Ankit, MNIT Jaipur
Dr. Dip P. Samajdar, IIITDM Jabalpur	Prof. Anand Bulusu, IIT Roorkee	Dr.J Ghosh, NIT Patna

Registration:
Registration is open to faculty, working professionals, industry persons, doctoral, postgraduate and graduate students. Participants will be admitted on first-come first-served basis.
Register online at– http://online.mnit.ac.in/eict/

Certification Fee: Academic (faculty/PhD scholars): Rs. 500/-
UG/PG students: Rs. 500/-
Working professionals, Industry/Others: Rs. 9500/-

(A) Fee once paid will not be refunded back.
(B) The fee covers online participation in the programme, tutorial notes and examination, certification charges.
(C) The organizers should receive the registration amount through online mode- NEFT/UPI, provided at the registration portal.
(D) Detailed schedule will be shared after receiving registration form.

→ For any other query, **email us at** fdp.academy@mnit.ac.in

MNIT Jaipur one of the oldest NITs, the institute has a rich heritage of sixty years producing world class engineers, managers, architects and scientists. Ranked 43rd nationally in the NIRF ranking-2024 (Engineering), the institute offers learning opportunities for undergraduate, postgraduate students, and researchers in various domains. Having a lush green campus of over 317 acres within the heart of the pink city, close to Jaipur International Airport, the campus offers a safe and lively environment. A world class teaching infrastructure, state-of-art laboratories welcome you at the campus. The institute has a vision to impart education of international standards and conduct research at the cutting edge of technology.