Jointly Organized by
Electronics & ICT Academy

MNIT Jaipur
http://www.mnit.ac.in/eict

Online/Classroom FDP on
VLSI Testing and Testability

14th July –18th July, 2025

Faculty Development Programme
Electronics & ICT Academy under aegis of

Ministry of Electronics and Information Technology
Government of India

meity.gov.in/content/schemes-projects

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Objective (Electronics & ICT Academy-Phase II)
1)To conduct specialized FDPs for faculty/mentor training in line with the vision of MeitY by promoting emerging areas of technology and other high-priority areas that are pillars of both the "Make in India" and the "Digital India" programs.
2) To promote synergy and collaboration with industry, academia, universities and other institutions of learning, especially in emerging technology areas.
3) To support the National Policy on Electronics 2019 (NPE 2019) which envisions positioning India as a global hub for ESDM sector, including MeitY Schemes/policies such as Programme for Semiconductors and Display Fab Ecosystem; India AI; National Programme on AI, Production Linked Incentive Scheme for IT Hardware & Large-Scale Electronics Manufacturing; EMC; SPECS; Chips to System (C2S); etc.
4) To promote standardization of FDPs through Joint Faculty Development Programmes.
5) To support the vision of the National Education Policy (NEP 2020), which mandates that Indian educators go through at least 50 hours in professional development programmes per year.
6) To design, develop & deliver specialised FDPs on emerging technologies/ niche areas/ specialised modules for specific research areas for Faculty in Higher Education Institutions (HEI), besides FDPs on multi-disciplinary areas connected with ICT tools and technologies and other digital hybrid domains, covering a wide spectrum of engineering and non-engineering colleges, polytechnics, ITIs, and PGT educators.

An intensive 40 Hours Training Programme in Online mode is being organized for faculty and doctoral students of engineering and technological institutions. It is also open to working professionals from industry/organizations. The main theme of the training program will be oriented around exploring the state-of-the-art methods for VLSI Testing and Testability.

Experts/Speakers-

Dr. C.P. Ravikumar, Texas Instruments Pvt Ltd
Mr. Deepak Agrawal, Vice President, HRDWYR,
Mr. Surendra kumar Tadi, Principal Manager, Qualcomm india pvt ltd
Mr. Prateek Mudgil, Engineering Manager, Synopsis Inc
Mr. Harshay Jaiswar, Sr Reliability Engineer, AMS OSRAM, Astria
Prof. Vineet Sahula, MNIT Jaipur
Dr. Menka Yadav, MNIT Jaipur
****Note: We are waiting a few more industrial experts' consents for this FDP.**

Programme Modules:

Introduction: Physical faults and their modeling. Fault equivalence and dominance; fault collapsing. Checkpoint Theorem. Fault simulation: parallel, deductive and concurrent techniques; critical path tracing. Combinational SCOAP Measures and Sequential SCOAP Measure. Critical Path Tracing

Test generation for combinational circuits: Boolean difference, D-algorithm, Podem, random etc. Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage. PLA testing: cross-point fault model, test generation, easily testable designs. Memory testing: permanent, intermittent and pattern-sensitive faults; test generation. Delay faults and hazards; test pattern generation techniques, ATPG and its different types

Test pattern generation for sequential circuits: ATPG for Single-Clock Synchronous Circuits, Use of Nine-Valued Logic and Time-Frame Expansion Methods, Complexity of Sequential ATPG , Scan Chain based Sequential Circuit Testing, ad-hoc and structures techniques scan path and LSSD, boundary scan Built-in self-test techniques: LBIST and MBIST.

Verification: logic level (combinational and sequential circuits), RTL-level (data path and control path). Verification of embedded systems. Use of formal techniques: decision diagrams, logic-based approaches. ASIC/IP Verification, direct and random testing, Error detection and correction codes.

Advanced research topics Research Trends, Challenges in VLSI Testing. Current Practices in VLSI Testing and Testability.

Programme Coordinator:

Dr.Menka Yadav fdp.academy@mnit.ac.in 9549650791(M)

Registration:

Registration is open to faculty, working professionals, industry persons, doctoral, postgraduate and graduate students from India and rest of the world. Participants will be admitted on first-come first-served basis. Register online at–(http://online.mnit.ac.in/eict/)

Registration Fee:

Mode of programme	Academia (faculty/Students): India/SAARC/Africa	Others: India/SAARC/Africa	Rest of the world
Online	Rs. 500/-	Rs. 1500/-	US $ 60/-
Classroom	Rs. 2000/-	Rs. 4000/-	--

(A) Fee once paid will not be refunded back.
(B) The fee covers online participation in the programme, tutorial notes and examination, certification charges etc.
(C) The registration amount may be paid through online mode- NEFT/UPI/Cards/SWIFT, provided at the registration portal.
(D) Detailed schedule will be shared after receiving registration form.

For any other query, email us at fdp.academy@mnit.ac.in

MNIT Jaipur one of the oldest NITs, the institute has a rich heritage of sixty years producing world class engineers, managers, architects and scientists. Ranked 43rd nationally in the NIRF ranking-2024 (Engineering), the institute offers learning opportunities for undergraduate, postgraduate students, and researchers in various domains.Having a lush green campus of over 317 acres within the heart of the pink city, close to Jaipur International Airport, the campus offers a safe and lively environment. A world class teaching infrastructure, state-of-art laboratories welcome you at the campus.The institute has a vision to impart education of international standards and conduct research at the cutting edge of technology.